# Benchmarking Semiconductor Manufacturing

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*Abstract*— **We are studying the manufacturing performance of semiconductor wafer fabrication plants in the US, Asia, and Europe. There are great similarities in production equipment, manufacturing processes, and products produced at these plants. Nevertheless, data reported here show that important quantitative measures of productivity vary by factors of 3 to as much as 5 across an international sample of 16 plants.**

**We conducted on-site interviews with manufacturing personnel to better understand reasons for the observed wide variations in productivity. We have identified factors in the areas of information systems, organizational practices, process and technology improvements, and production control that correlate strongly with productivity.**

## I. Introduction

THE Competitive Semiconductor Manufacturing (CSM) Program at the University of California, Berkeley, since April 1991, has been conducting a detailed study of quality, productivity, and competitiveness in semiconductor manufacturing worldwide. The program is a joint activity of the College of Engineering, the Haas School of Business, and the Berkeley Roundtable on the International Economy at Berkeley, under sponsorship of the Alfred P. Sloan Foundation, and with the cooperation of semiconductor producers from Asia, Europe and the United States. The authors of this paper are the project's Co-Directors. Other contributors are named in the Acknowledgments. This article is based on data and analysis drawn from the continuing program [1].

The CSM program is being conducted by faculty, graduate students and research staff from UC Berkeley's schools of Engineering and Business, and Department of Economics. Many of the participating firms are represented on the program's Industry Advisory Board. The Board played an important role in defining the research agenda. A pilot study was conducted in 1991 with the cooperation of three semiconductor plants. The research plan and survey documents were thereby refined. The main phase of the CSM benchmarking study began in mid-1992 and will continue at least through 1997.

## II. Focus of this Study

Our study focuses on semiconductor wafer processing as needed to produce VLSI chips including memories, microprocessors, signal processors, other logic, and mixed-signal products. Wafer processing takes place in manufacturing plants known as "fabs". Modern fabs require capital investment in plant and equipment of $500M to $1B each. They are the most costly manufacturing plants found in any industry today. The knowledge and skills required for efficient wafer fabrication require further large, ongoing investments. Manufacturing process sequences are exceedingly complex, with 400 or more sequential operations on a wafer over a span of 20 to 60 24-h days. A gross failure at any step can render a wafer worthless. The salable fraction of the total number of chips on a finished wafer, known as the "chip yield," varies from zero to 100%, depending on the effectiveness of quality control in avoiding localized defects on chips.

Today's principal VLSI products including memories, microprocessors, digital signal processors, application-specific logic, etc. are manufactured worldwide using very similar manufacturing equipment and processes. In many cases, 5 to 15 firms world-wide compete in selling interchangeable final products to hundreds of customers. Economic success in wafer fabrication clearly requires maximizing the output of salable products from a large fixed investment. Despite these obvious facts, there is an amazingly large variation in the manufacturing performance of semiconductor firms. The present study is intended to quantify and benchmark manufacturing performance and to identify superior practices in manufacturing technology, factory operation, organization, and management.

Our study has addressed only the wafer fabrication element of the total semiconductor manufacturing cycle. This is the most complex and capital-intensive element. The technologies and processes of packaging semiconductor chips are, however, growing in significance. Semiconductor packaging is the subject of a forthcoming report from another group [2].

## III. Sources of Data and Limitations on Its Disclosure

The data and analysis summarized in this report derive from measurements of manufacturing performance and investigation of underlying determinants of performance at 16 wafer fabrication facilities in the United States, Europe, Japan and Taiwan. The companies operating these manufacturing facilities are listed in Table I. In selecting participants, we sought access to plants representing a cross-section of the industry, both internationally and in terms of business models and product mix. We asked for access to plants that had been in operation for at least three years. Substantial effort is required on the part of each participant. Some of those approached declined to participate. Participants who operate several semiconductor manufacturing lines generally opened one of their best lines to this study. Firms participate based on written agreement that we mask the relationship between individual firms and plants. We report results only in anonymous or aggregated forms.

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TABLE I
COMPANIES PARTICIPATING IN THE MAIN PHASE OF THE COMPETITIVE SEMICONDUCTOR MANUFACTURING SURVEY (FIRST 18 MONTHS)

| | |
|---|---|
| Advanced Micro Devices, Inc. | Nihon Semiconductor, Inc. |
| Cypress Semiconductor, Inc. | NEC Corp. |
| Delco Electronics, Inc. | Oki Electric Industry, Ltd. |
| Digital Equipment Corp. (2 sites) | Silicon Systems, Inc. |
| Intel Corporation | Taiwan Semiconductor Mfg. |
| International Business Machines, Inc. | Texas Instruments, Inc. |
| ITT Intermetall | Toshiba Corp. |
| LSI Logic. Corp | |

The Berkeley team signs nondisclosure agreements with all participating firms.

As the first step, participants complete a 70–page mail-out questionnaire (MOQ), reporting data concerning clean room size and class, staffing levels, equipment counts, wafer starts, die yields, line yields, cycle times, manufacturing systems, etc. over the last four years. From the completed MOQ's, we calculate technical metrics of manufacturing performance for each participant. We then rank the participants for each of the metrics.

We observed a great variation in the scores. In an attempt to understand the factors that account for performance differences, we conduct a two-day visit at each participating site. We tour the manufacturing line, interview a cross-section of the staff, and hold a series of sessions to determine the fab's strategies for improving manufacturing performance. We assess each fab's resources for improvement including computer integrated manufacturing (CIM) and information systems, human resources development, deployment of work groups and teams, etc. These more qualitative evaluations of participants' operational practices are then correlated with the performance metrics to identify those practices that underlie top performance.

## IV. METRICS OF MANUFACTURING PERFORMANCE

The technical metrics we use to measure manufacturing performance of the participants are defined as follows:

1) *Cycle time per wafer layer* measures the duration, expressed in fractional working days, consumed by production lots of wafers from the time of release into the fab until time of exit from the fab, divided by the number of masking layers. The participants report cycle times for each of several process flows they may operate; we compute a weighted average cycle time per layer for the fab, where the weights are the number of wafer starts in each process flow.
2) *Line yield* measures the fraction of wafers started that emerge from the fab as completed wafers ready for electrical testing of the individual circuits on the wafer. In monthly periods, the participants report line yield for each of their process flows, calculated as

$$(\mathrm{WO})/[(\mathrm{WO}) + (\mathrm{SC})]$$

where WO is the number of wafers completed during the month and SC is the number of wafers scrapped during the month. We normalize the reported line yields into scores expressing the line yield per ten wafer layers using the formula

$$\mathrm{LY10} = \mathrm{LY}^{(10/\mathrm{ML})}$$

where LY is the reported line yield, ML is the number of masking layers, and LY10 is the calculated line yield per ten layers. We then compute a weighted average line yield per ten layers for the fab, where the weight for each process flow is the number of wafer starts of the flow.
3) *Die yield* expresses the fraction of the total whole die on a completed wafer that pass the electrical probe test. The participants report their die yields for the highest volume product in each of their process flows. For memory products, the reported die yield is that after laser repair. We convert the reported die yield into a defect density using the Murphy model

$$Y = \{(1 - e^{-AD})/AD\}^2$$

where $Y$ is the reported die yield, $A$ is the die area in square centimeters, and $D$ is the calculated defect density, expressed as defects per square centimeter. The calculated defect densities account for all yield losses remaining after repair, including spot defects, parametric problems, and any other losses. We compare defect density scores of the participants only after sorting process flows into memory and logic groups that are further categorized by the minimum geometry achievable with the flow.
4) *Stepper productivity* expresses the number of wafer layers completed per 5X stepper per calendar day (considering only layers exposed using 5X steppers). We estimate the number of wafer operations in a process flow performed per calendar day by 5X steppers using the formula

$$\mathrm{SL} = (\mathrm{WS}/7)(\mathrm{NL})(\mathrm{LY}')$$

where SL is the calculated number of 5X stepper operations per day, WS is the reported average number of wafer starts per week in the process flow, NL is the number of masking layers in the process flow performed on 5X steppers, and LY′ is an inflated line yield computed as

$$\mathrm{LY}' = (1.0 + \mathrm{LY})/2$$

where LY is the reported line yield for the process flow. (This inflated line yield allows for half of the total line yield loss to load 5X steppers, or equivalently, it assumes the average wafer that is scrapped makes it through half the 5X layers before being discarded.) The calculated 5X stepper operations per day for all process flows are summed, then divided by the number of 5X steppers present in the fab to obtain the value of the metric.
While participants processing a wide variety of products must change reticles more frequently than those producing only a few products, we observed that some participants have automated reticle changes to the point that there is almost no lost time on their 5X steppers when they change reticles. We therefore make no al-

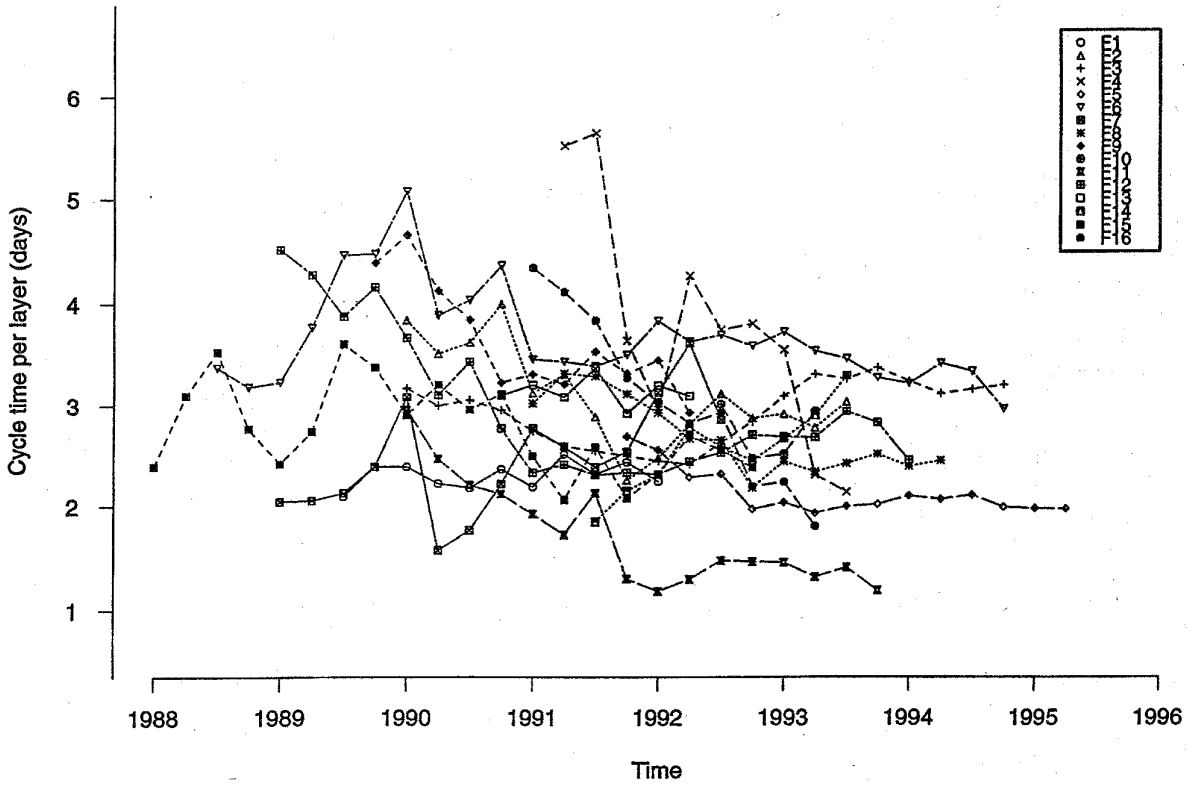



Fig. 1. Cycle time per layer.

lowance for product mix in computing this metric. We also did not make any allowances for differences in average die sizes among the participants.

5) *Direct labor productivity* expresses the total number of wafer layers completed per operator per working day. To compute this metric, we first estimate for each process flow the total number of wafer layers completed per working day using the formula

$$\mathrm{WL} = (\mathrm{WS}/\mathrm{WD})(\mathrm{TL})(\mathrm{LY}')$$

where WS is the average number of wafer starts per week, WD is the number of working days per week, TL is the total number of wafer layers in the process flow, and LY′ is the inflated line yield defined as above. We then compute the metric by summing the WL figures for each process flow and dividing by the reported number of production operators.

6) *Total labor productivity* expresses the total number of wafer layers completed per working day divided by the total head count. This metric is computed similarly, except the divisor is the reported total number of fab employees, including dedicated staff from equipment vendors.

7) *On-time delivery* measures the ability of the participants to meet production schedules. It expresses the percentage of items scheduled for output in a week whose actual output quantity by the end of the week is greater than or equal to the scheduled quantity. Some participants report on-time delivery at the die level, some at the finished goods level, some at both levels, while others declined to state their performance or simply did not know.

We encountered a wide range in scores for each metric, even though the basic process technology and the major manufacturing equipment in use at the participants were generally similar. Table II summarizes the best, average, and worst scores for each metric, considering the latest data points we received from each of the sixteen participants, and provides an estimate of the relative ranking of Japanese and US firms in each metric. These data points represent measurements of manufacturing performance in some quarter between the middle of 1992 and the end of 1993, depending upon the participant.

Rates of improvement also are studied for each participant. Figs. 1–6 graph the first six metric scores over time for the participants. To protect confidentiality, a coding scheme is used whereby the participating fabs are labeled $F1$–$F16$. The scheme is uniform across the graphs, e.g., $F1$ refers to the same fab on all graphs. Scores for each technical metric are computed for each quarter over a period of three to four years. In graphs of defect densities, multiple curves are sometimes displayed for the same fab, indicating the fab operated more than one process flow in the category of flow that is graphed. For most metrics, the ranking of participants does not change quickly. We did not find many cases where a last-place participant overtook the leader for a particular metric, although a few participants improved their rankings considerably over the period.

Perhaps the most striking phenomenon observed in our measurements concerns the initial defect densities for process

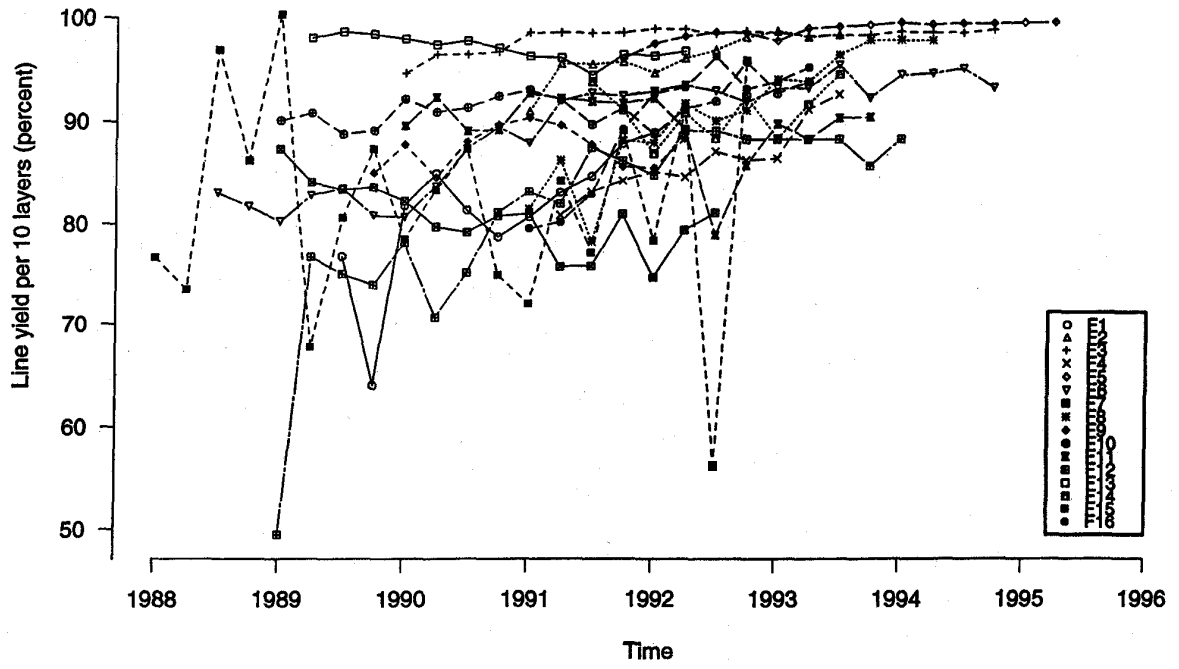



Fig. 2. Line yield.

flows, that is, the defect densities realized in the first quarter after transfer of the process flow into manufacturing. We recorded a factor-of-ten range in initial defect densities. Those fabs with poor starting points tend to have faster rates of improvement, but not nearly fast enough to overtake those with good starting points, at least not for several years, as those with good starting points also make steady if somewhat slower progress reducing defect densities.

## V. Analysis of Practices Underlying Manufacturing Performance

Our main objective in the CSM survey is to identify those operational practices that underlie leading-edge manufacturing performance. Summarized below are the operational practices that distinguish those fabs achieving best or near-best scores in one or several of the metrics described above. (For the sake of brevity, we refer to such fabs as the "leading" fabs.) But before summarizing our findings in that regard, it is only fair to acknowledge that our analysis does not account for several strategic factors concerning product design and fab design that may strongly influence manufacturing performance.

First, the restrictiveness of product design rules can have a strong influence on observed die yields and hence on our calculated defect densities. Issues of overall business strategy influence the choice of design rules and affect the priority attached to the different metrics of manufacturing performance. We made no attempt to normalize defect density scores for differences in design rules and/or overall business strategy among the participants.

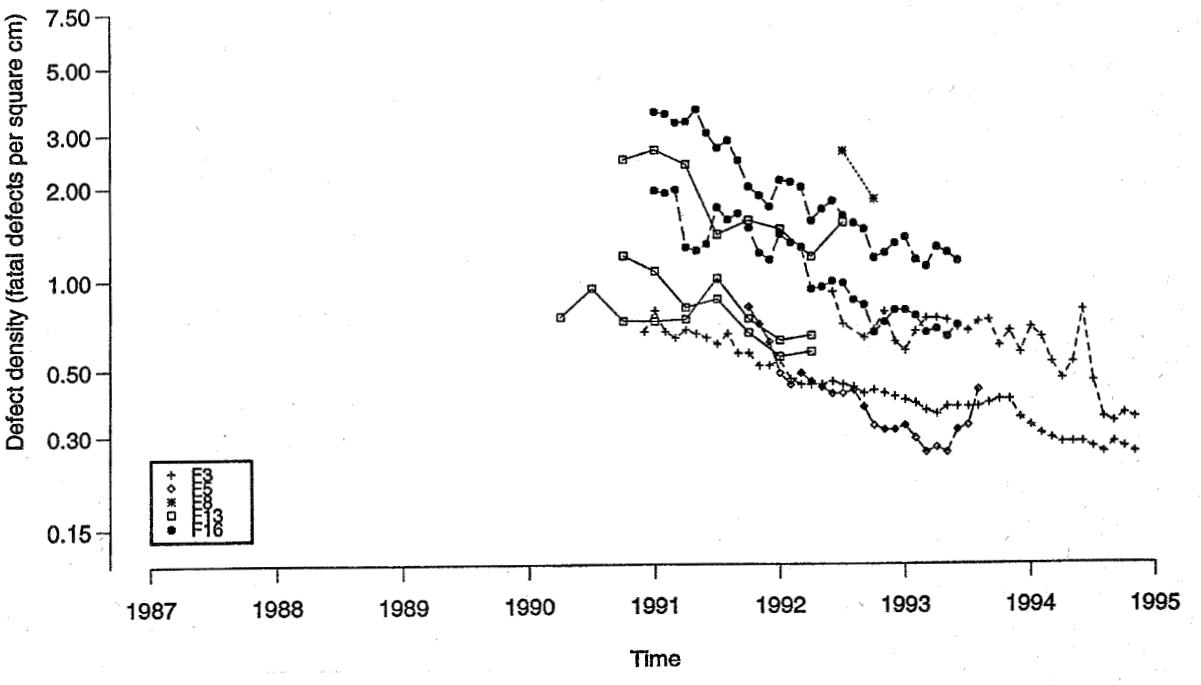
Second, the range of sizes of fabs in our survey, in terms of wafer starts, spans a factor of almost fifty. Small fabs generally have inferior labor and equipment productivity scores, because of the indivisibility of machines and operators, and because of the tendency to install extra equipment to avoid situations in which a particular process step must be performed by a one-of-a-kind equipment type. We made no attempt to normalize productivity scores to account for fab size.

Third, the assignment of older-generation of processing equipment to newer-generation process flows may result in lower values for several metrics than would be possible with newer equipment. While yields may be lower for the strategy to employ older processing equipment, capital costs are lower

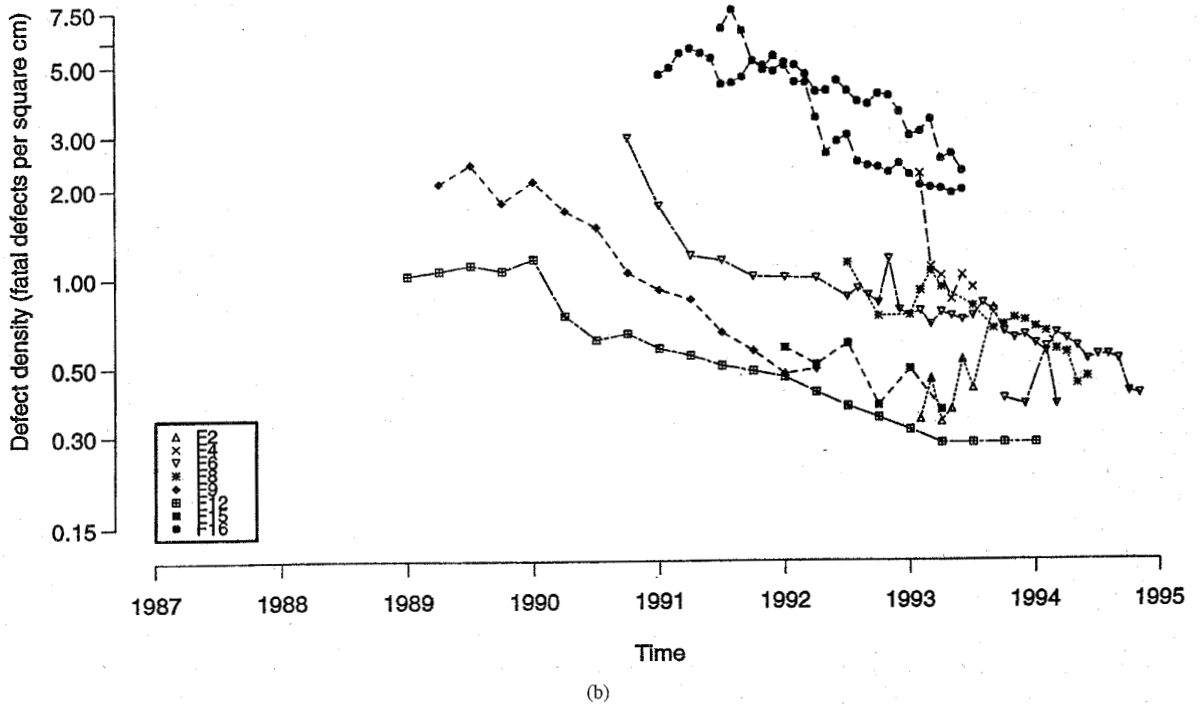
TABLE II
Summary of Technical Metric Scores, Competitive Semiconductor Manufacturing Survey (First 18 Months)

| Metric | Best score | Average score | Worst score | Japan vs. US |
|---|---|---|---|---|
| Cycle time per layer (days) | 1.2 | 2.6 | 3.3 | – |
| Line yield per ten layers (%) | 98.9 | 92.8 | 88.2 | ++ |
| Murphy defect density - ($defects/cm^2$) | | | | Overall: ++ |
| 0.7 - 0.9 micron CMOS memory | 0.28 | 0.74 | 1.52 | |
| 0.7 - 0.9 micron CMOS logic | 0.28 | 0.79 | 1.94 | |
| 1.0 - 1.25 micron CMOS logic | 0.23 | 0.47 | 0.96 | |
| 1.3 - 1.5 micron CMOS logic | 0.21 | 0.61 | 1.15 | |
| 5X stepper throughput (5X layers completed per machine-day) | 724 | 382 | 140 | + |
| Direct labor productivity (wafer layers completed/operator-day) | 63.0 | 29.6 | 8.0 | + |
| Total labor productivity (wafer layers completed/total staff-day) | 37.7 | 17.6 | 3.3 | ++ |
| On-time Delivery (% of line items with 95% of die output on time) | 100% | 89% | 76% | – |

Average and worst scores are calculated after discarding the worst data sample for each metric. Legend:
++ Japanese fabs are almost uniformly superior
+ Japanese fabs are generally superior
0 Superior/inferior fabs are not distinguished by region
– US fabs are generally superior
— US fabs are almost uniformly superior




(a)



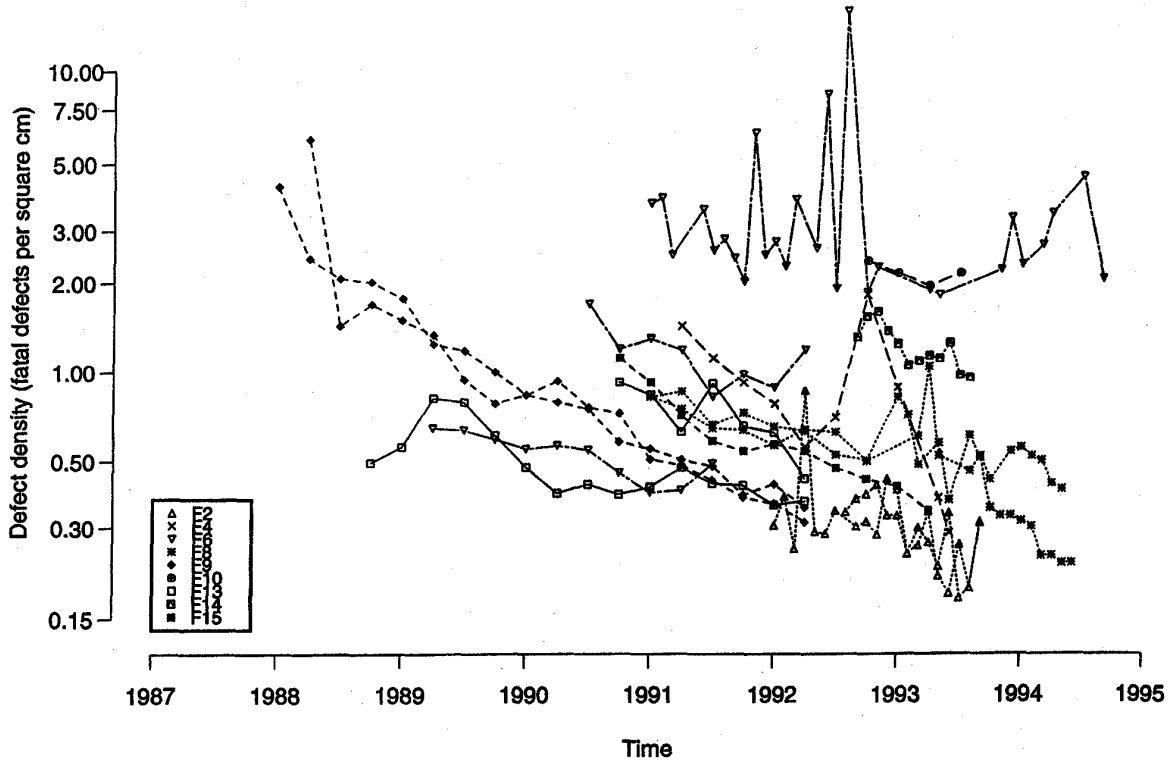

(b)

Fig. 3. (a) Memory defect density 0.7–0.9$\mu$ CMOS process flows. (b) Memory defect density 0.7–0.9$\mu$ CMOS process flows. (c) Logic defect density 0.7–0.9$\mu$ CMOS process flows. (d) Logic defect density 1.3–1.5$\mu$ CMOS process flows.

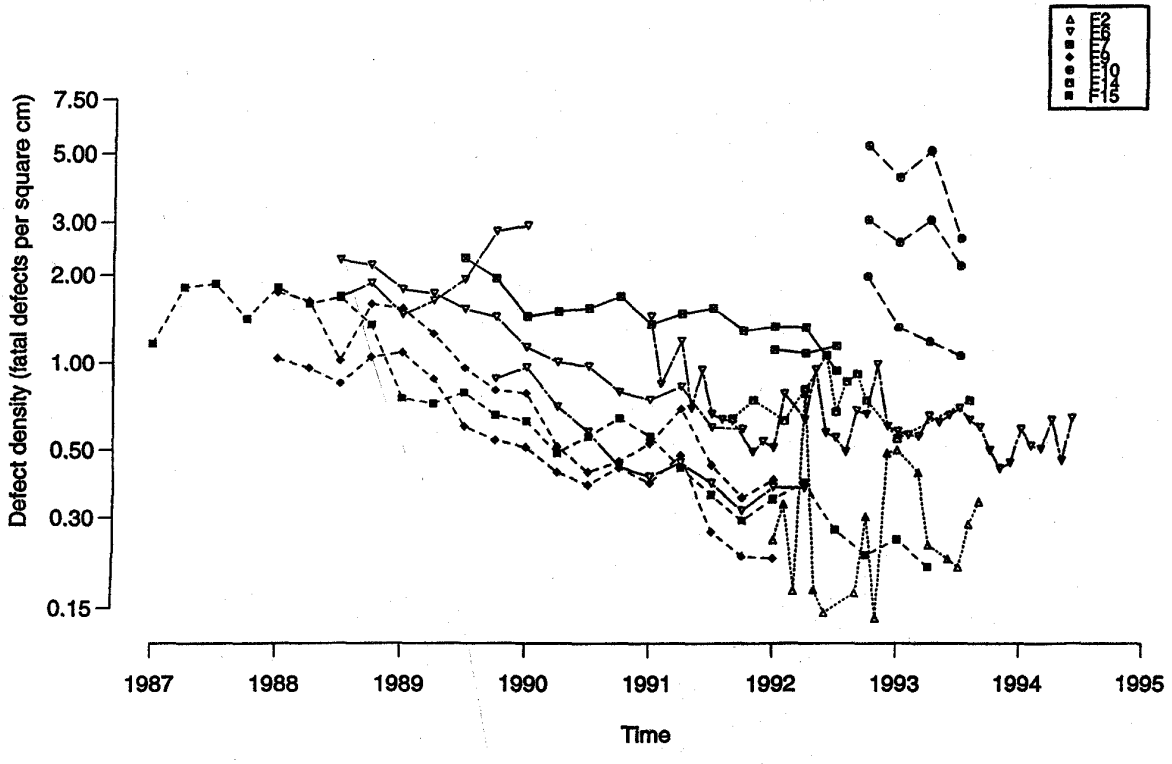
as well, and so the strategy might turn out to be economically competitive or even superior to the strategy that employs solely new processing equipment. We made no attempt to normalize metric scores for the generations of equipment applied.

With these strategic factors aside, we now turn to the various operational practices we found to be correlated with good manufacturing performance (in terms of the manufacturing metrics we have defined). These practices may be categorized into four basic types of practices at which a fab must excel in order to realize excellent manufacturing performance.

First, a fab must have computer systems providing strong process control, excellent data collection and excellent data




(c)




(d)

Fig. 3. (*Continued.*)

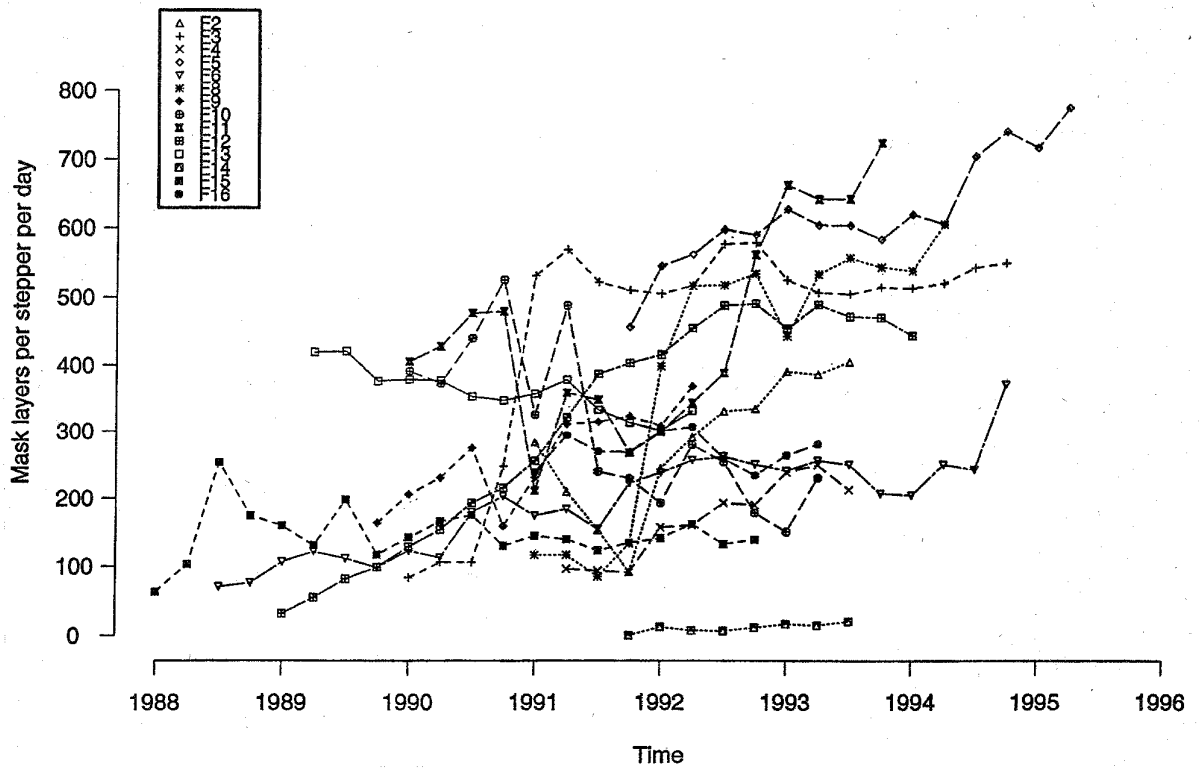



Fig. 4. 5X stepper productivity.

analysis capabilities. The fab must be able to expeditiously pinpoint the causes of yield loss and the sources for losses of wafer throughput. The fab must be able to promptly recognize when processing is being done incorrectly, or better yet, prevent misprocessing entirely with equipment and system controls and procedural checks.

Second, a fab must have an organization that not only executes the manufacturing processes well, but also is very good at problem recognition and at problem solving. Semiconductor manufacturing is characterized by immature processes and immature processing equipment with relatively short lives, and by continuing increases in complexity. Opportunities to improve yields and/or wafer throughput are always present. Thus manufacturing has a major engineering element as well as an operational character. This means a fab must continually improve the technical competence of its organization and continually foster a teamwork approach to recognize problems, devise innovative solutions, and implement them quickly and successfully. Not only engineers but also operators and technicians must participate in problem recognition, process improvement and problem solving, and they therefore must possess basic engineering skills as well as technical knowledge of the manufacturing processes and equipment.

Third, and closely related to the second area, the fab must have the internal technical talent as well as the requisite support from vendors to expeditiously make modifications to product, process, and equipment in order to implement changes that have been identified by problem-solving efforts as desirable or necessary to improve manufacturing performance.

Fourth, and finally, a fab must have effective procedures for managing the introduction of new process flows. The economic life of many process flows is three to four years, with unit prices for products of the flow declining rapidly over this period. Thus it is economically important to realize high throughput of the process flow early in its life, and to fairly frequently introduce new process flows into the fab. This means the fab must become expert in each new process flow and its required equipment as soon as possible, ideally before it transfers to production, so as to realize good yields and good wafer throughput early in its life and to quickly ramp to better yields and higher wafer throughput thereafter. Even if a fab is proficient in the above three types of practices, a poor start with a new flow may leave the fab too far behind to catch up before the market value of the output has mostly drained away.

Table III provides a tabulation of particular operational practices of these types, the impacted metrics, and comparisons of the overall rankings for Japanese vs. U.S. manufacturers. These rankings include some weight added in recognition of the intensity or effectiveness of practice. As can be seen, the practices are organized into categories titled CIM and Information Systems, Organizational Practices, Formal Procedures, Process and Technology Improvements, and Production Control.

## VI. CIM and Information Systems

In the area of CIM and Information Systems, the leading fabs collect and analyze large amounts of data, enabling them to trouble-shoot their manufacturing processes and equipment

TABLE III
SUMMARY OF EFFECTIVE MANUFACTURING PRACTICES

| Practice | Metrics Influenced | Japan vs. US |
|---|---|---|
| ***CIM and information systems*** | | |
| SPC | Defect Density, Line Yield | ++ |
| Equipment efficiency measurement | Equipment throughput, cycle time, labor productivity | ++ |
| Visual displays of SPC charts, equipment tracking, etc. | Line yield, defect density, labor productivity, equipment throughput | + |
| Automation of data logging | Cycle time, defect density, labor productivity, equipment throughput | ++ |
| Auto recipe download and/or display | Line yield, cycle time, defect density, labor productivity, equipment throughput | 0 |
| Automated feedback control at photolithography | Defect density | 0 |
| Yield correlation analysis | Defect density | ++ |
| In-line electrical measurements | Defect density | + |
| In-line particle measurements | Defect density | + |
| Automated trouble messaging and automated assistance for trouble-shooting | Cycle time, line yield, equipment throughput, labor productivity | - |
| ***Formal Procedures*** | | |
| Formal procedures for new process introductions | Defect density, line yield, equipment throughput | ++ |
| TPM program | Equipment throughput, cycle time, line yield, defect density, labor productivity | ++ |
| ***Organizational Practices*** | | |
| Exchange of engineers with development fab | Defect density, line yield, equipment throughput | ++ |
| Integration of engineering groups | Defect density | ++ |
| Integration of engineering and manufacturing staff | Equipment throughput, line yield, defect density | ++ |
| Operator and technician improvement teams | Equipment throughput, cycle time, line yield | ++ |
| Mentoring by senior engineers and supervisors | Defect density, line yield, equipment throughput | ++ |
| Mentoring by senior operators | Line yield, cycle time, equipment throughput | ++ |
| Extensive leadership training | Defect density, line yield, equipment throughput | ++ |
| "Stretch" goals | Defect density, line yield, equipment throughput, labor productivity | ++ |
| ***Process and Technology Improvements:*** | | |
| Machine modifications to automate load/unload or wafer handling mechanisms | Line yield, cycle time, labor productivity, equipment throughput | ++ |
| Machine modifications to reduce particle counts | Defect density, cycle time, labor productivity, equipment throughput | ++ |
| Process flow re-design | Defect density, cycle time, line yield, equipment throughput | + |
| Product re-design | Defect density | ++ |
| Machine lights and audio alarms | Cycle time, equipment throughput, labor productivity | ++ |
| Linked photolithography cells | Defect density, cycle time, equipment throughput | 0 |
| Automated interbay lot movement | Cycle time, labor productivity | ++ |
| ***Production Control*** | | |
| Kanban | Cycle time, labor productivity | -- |
| Computerized dispatching | Cycle time, labor productivity, on-time delivery | -- |
| Production planning based on measured equipment capacity | On-time delivery | -- |

Legend: ++ Japanese fabs are almost uniformly more effective
+ Japanese fabs are generally more effective
0 The most effective practitioners are not distinguished by region
- United States fabs are generally more effective
— United States fabs are almost uniformly more effective

quickly and comprehensively. All participants in our study have embraced statistical process control (SPC) as a means of detecting manufacturing problems and improving process performance. Almost all provide automated notification of out-of-control conditions. The leading fabs rigorously manage their SPC programs, retiring unneeded control charts and adding new ones recognized as desirable, adjusting control limits as appropriate, adjusting frequencies of measurements to focus efforts on the most critical areas, and maintaining an effective training program.

SPC measurements are made both of product wafers and of machine conditions, such as particle counts of machine exhaust flows or of blank wafers passed through the machine. The leading fabs have information systems that automatically provide assistance for responding to out-of-control situations, such as auto-display of corrective action guidelines, automatic disabling of equipment or process, automatic notification of the responsible engineers, etc. SPC measurements also are used to trigger preventive maintenance and tool or material replacements.

All of our participants have engineering databases to which they upload some amount of metrology data, SPC measurements, and production tracking data (such as which machine was used to process a lot, which operator attended to it, which batch of chemicals was used, etc.). The leading fabs upload more data, and they have automated the upload of much of these data using bar codes or magnetic cards and sensors.

The top fabs efficiently perform end-of-line yield analyzes by integrating their engineering database with the database of die yields and parametric measurements taken at the end of the manufacturing line. Automated statistical correlations are made between die yield results and the data uploaded to the engineering database described above, in order to ascertain what characteristics are common to low-yielding

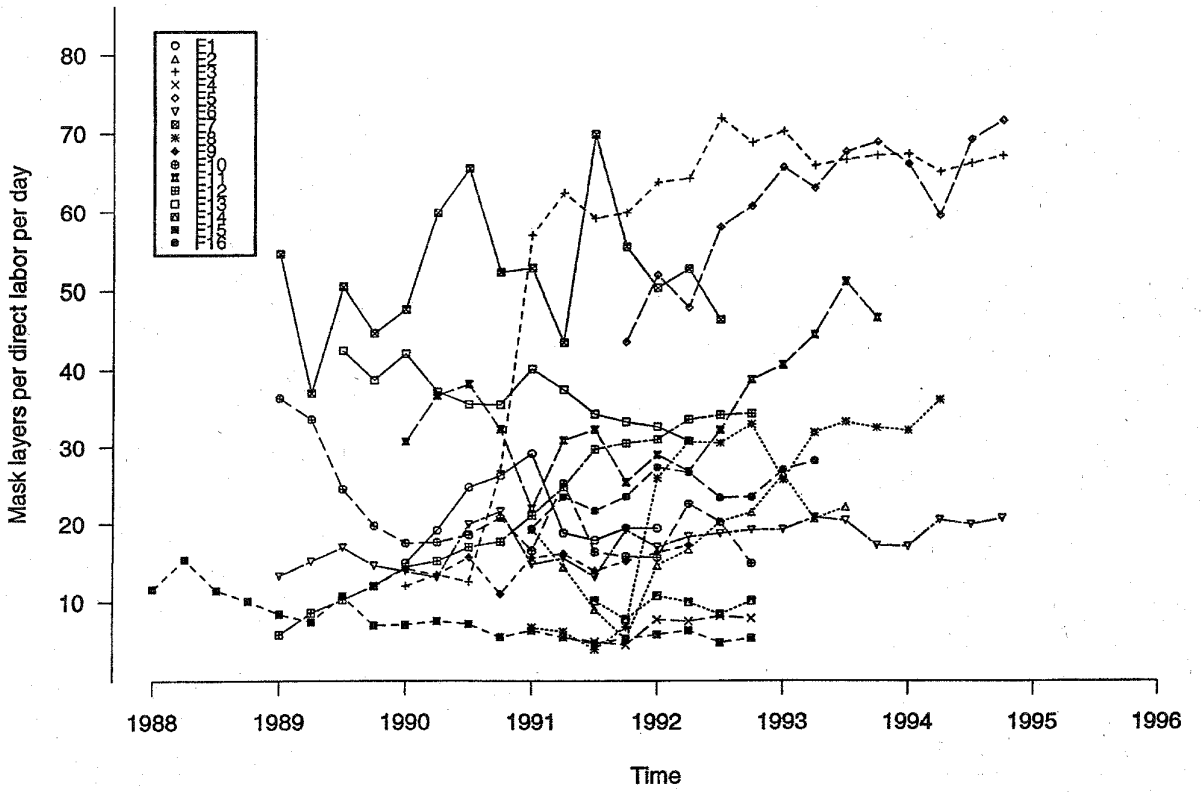



Fig. 5. Direct labor productivity.

wafers. Leading fabs feature yield improvement groups that build yield models specifically for their fab, perform extensive wafer map analysis of yield patterns to find clues to the types of processing equipment where losses were incurred, as well as carry out statistical correlation analyzes as described above. The leading fabs document their findings for each major event of yield loss, and save these findings in a database for future reference.

Leading fabs also are increasing their efforts for in-line yield analysis using digital image processing and laser scanning machines to conduct particle inspections of partially-processed wafers. Wafer maps showing the distribution of particles are classified so as to obtain clues concerning the equipment source of the particles; SPC procedures are instituted for particle inspections, for which out-of-control incidents trigger partitioning analyzes to pinpoint the source of particles; and end-of-line die yields are statistically correlated with in-line particle measurements of the product wafers.

The leading fabs make effective use of computers to prevent processing errors. Automated recipe download is installed at most or even all processing equipment in leading fabs. "Smart" lot-machine interfaces have been installed by some leading fabs, whereby the computer system prevents one from tendering the wrong lot or the wrong recipe to the machine. In addition, "smart" lot and reticle racks also are used at one participant to highlight the correct lot and reticle to be used. A couple of leading fabs also have automated the feedback control of photolithography exposures based on critical dimension measurements.

## VII. Organizational Practices

In the area of organizational practices, the leading fabs practice considerable integration of sustaining engineering staff with development engineering staff in order to make the introduction of new process flows more successful. The top fabs exchange engineers with the development fab that is the source for their new process flows, sending their own engineers to development before time of transfer, or receiving engineers from development at time of transfer, or both. Considerable engineering hours are invested in the transfer of a new process technology rather than merely in its development. For example, at a number of leading participants, the development fab will continue to run the new process in parallel with the production fab for some period of time in order to provide equipment backup and useful reference data. These steps are taken to ensure the fab has expertise in new process flows right from the moment they enter production, as well as to ensure that new flows and their associated processing equipment are installed, configured and operated to provide the desired results.

The leading fabs have organized the various types of sustaining engineers into more integrated departments of product engineers, process engineers and equipment engineers so as to promote interdisciplinary problem-solving and shared accountability. This integration of what are traditionally distinct engineering groups comes from the recognition that solving yield and throughput problems requires a variety of expertise as well as consideration of many trade-offs, and that specialists

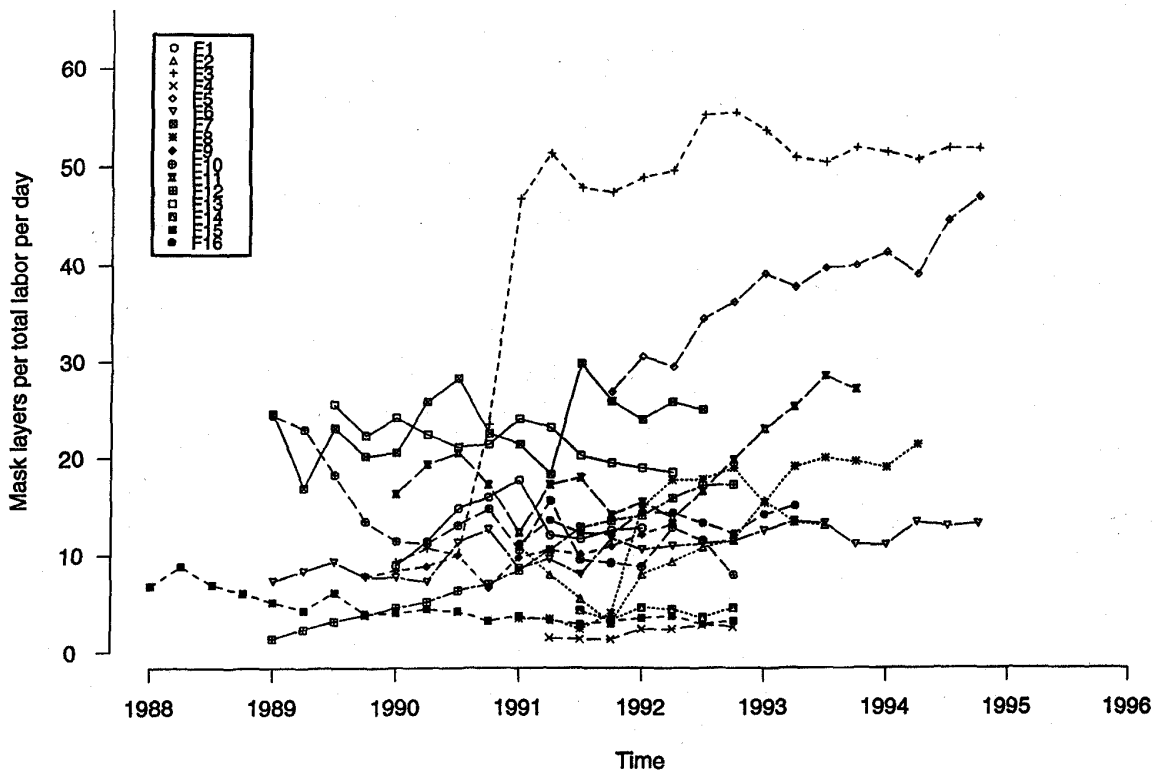



Fig. 6. Total labor productivity.

in one engineering area will benefit from increased knowledge of related areas. These integrated organizations also feature substantial efforts to mentor technical staff to higher levels of responsibility and higher levels of technical knowledge, e.g., mentorship of junior engineers by senior engineers, mentoring of technicians by engineers, etc.

At leading fabs improvement projects are not merely the domain of engineers. Improvement teams of operators and technicians are formed and guided by managers and engineers to address and solve manufacturing problems appropriate to their knowledge and experience. This team activity at leading fabs is an essential strategy for training employees and for upgrading their skill and knowledge levels. Umbrella programs such as TQM and TPM are used effectively as a means of rallying and focusing team efforts, and especially for training in formal methodologies for problem-solving. The leading fabs have very large numbers of improvement teams, with nearly every technician and operator involved in improvement projects. Virtually all technicians and even many operators are sent to classes run by equipment vendors in order to increase their equipment knowledge.

TQM (Total Quality Management) focuses improvement efforts on product quality. TPM (Total Productive Maintenance) focuses improvement efforts on equipment productivity. The two paradigms are thus complementary, and tend to drive different kinds of improvements. While most of the leading fabs had embraced TQM first and then TPM later, this is probably a historical artifact reflecting the relative ages of the paradigms.

The resulting acquisition of skills and knowledge leads to a more productive division of labor in leading fabs. Operators in leading fabs perform preventive maintenance and minor repairs of processing equipment, help design SPC charts, and participate in trouble-shooting efforts following formal methodologies. Technicians are thus freed to focus on major maintenance and repairs, improvement projects, training, and the documentation of equipment-related procedures. In turn, engineers are freed to focus most of their time on major improvement projects rather than on trouble-shooting exercises.

The leading fabs engage in extensive mentoring and employee development at all levels, with senior managers developing managers, senior engineers developing the engineers working with them, right down to senior operators and technicians developing operators in each equipment bay. In lieu of hiring professional supervisors, leading fabs promote experienced line workers to positions as group leaders, where their knowledge and experience makes them suitable to serve as mentor to workers in their area. At these fabs, there is extensive and continuing leadership training for engineering and manufacturing managers, all the way up to the executive officers. Our program has issued a report that gives detailed comparisons of human resources practices in semiconductor manufacturing [4].

Not only do the leading fabs establish programs for continuous improvement, they also set ambitious stretch goals for improvements in productivity and quality that force systemic improvements, and they do extensive technical planning, project and team planning and mentoring to realize those

goals. Many of the factors just mentioned closely parallel successful practices of world leaders in automobile assembly, as described in [3].

In the area of formal procedures, the leading fabs have established formal procedures governing the transfer and introduction of new process flows. There also are efforts at leading fabs to modularize process design, whereby new processes make use of proven modules from previous-generation processes, where feasible to do so. Such procedures serve to maximize the likelihood that new processes provide favorable yields in the first quarter of production, and that volume may be ramped quickly.

While all of our participants use SPC as a formal procedure for in-line measurement of quality, and all of our participants make efforts to measure equipment availability and utilization, the leading fabs have formal procedures for the measurement of true equipment productivity rather than merely its utilization. The leading fabs also have formalized the improvement of procedures for equipment maintenance, operation, analysis and training under the TPM paradigm.

## VIII. Process and Equipment Improvements

In the area of process and equipment improvements, the leading fabs make useful modifications to processing equipment to reduce downtime, to reduce particles, to reduce wafer breakage or scratches, to reduce handling, to reduce machine setups, to reduce the need to process test or pilot wafers, and to reduce unit processing times. They have the necessary expertise on-site, they obtain support from equipment vendors as required, and they have an organizational structure that integrates process and equipment engineers so as to deduce the most prudent equipment modifications to make considering the desired process characteristics. The leading fabs have installed lights and audio alarms on the processing machines to focus attention on idle or malfunctioning machines. Photolithography at the leading fabs is performed in linked cells achieving superior die yields, low rates of rework, low cycle times and high throughput.

Sometimes, modifying the equipment is not the most effective solution to a yield problem. The leading fabs also make changes to product designs or process flows for increased manufacturability. Such changes reflect an organizational structure that integrates product, process and equipment engineers, enabling them to identify and make trade-offs between potential equipment and product changes.

## IX. Introduction of New Processes and Products

Fig. 3(a)–(d) make it clear that manufacturing defect density at the time first production product is shipped to customers varies by a factor of 5 to 10 among the fabs studied. While learning rates for defect density vary somewhat, rarely is a bad start overcome by subsequent rapid improvement. This observation underlines the critical importance of highly disciplined development activity, and of tight coupling between development and manufacturing when the transfer takes place. The best performers accomplish successful new process introductions with temporary or permanent transfers of key personnel.

Special mention should be made of the application of standard mechanical interface (SMIF) technology, involving the implementation of portable micro-environments for processing equipment and lots [5]. We saw one participant, using an older and much more modest clean room than other participants operating comparable process flows, obtain world-class die yields. The introduction of SMIF technology clearly extended the economic life of this older fab and thus constitutes a very good technological improvement. The isolation of each machine from the rest of the fab also facilitated staged and selective upgrading of the equipment set in the fab.

Special mention also should be made with respect to the leading fab in terms of cycle time. Over several years, this fab has steadily rearranged its layout to break up the standard farm-type layout in favor of smaller cells of equipment handling a smaller variety of operation sequences. While in the past cell-type layouts have been resisted by many fab designers for fear of lost equipment utilization, this same fab is also our leader in 5X stepper throughput. This fab has demonstrated that a more cell-type layout represents a technological improvement, in that cycle times can be reduced while achieving leading-edge equipment throughput.

Finally, in the area of production control, the leading fabs perform automated production planning based on measured equipment capacity and cycle times to achieve high levels of on-time delivery. Re-planning is performed frequently and swiftly to keep up with revised intelligence on market demand and customer orders. On the factory floor, both Kanban and computer-assisted dispatching (lot sequencing) are used by leading fabs to improve cycle time as well as on-time delivery.

## X. Summary

Japanese plants examined as a part of our semiconductor manufacturing study on the whole are more effective in implementing preferred manufacturing practices. Management and workers share a firm commitment to continuing improvements. As a consequence, quality and productivity measures for those plants are excellent and improve steadily. While a few US plants achieve similar excellence, many US plants in our survey fall far behind the leaders in these categories. On the other hand, US plants are generally more effective in terms of cycle time and on-time delivery performance.

Our prescription for improved US manufacturing competitiveness calls for the high quality management and leadership frequently exhibited by US firms in research, product definition, finance, and marketing to be matched in manufacturing. While some readers may wonder if there may be social, cultural or legal barriers inhibiting implementation in US plants of leading-edge organizational practices described in this paper, we find nothing particularly "Japanese" about them. Indeed, the US plants achieving excellence similar to our Japanese participants tend to exhibit similar organizational practices.

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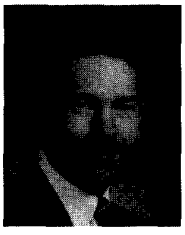

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